Interconnect Reliability under ESD Conditions: Physics, Models, and Design Guidelines

Kaustav Banerjee

Center for Integrated Systems
Stanford University
http://ee.stanford.edu/~kaustav

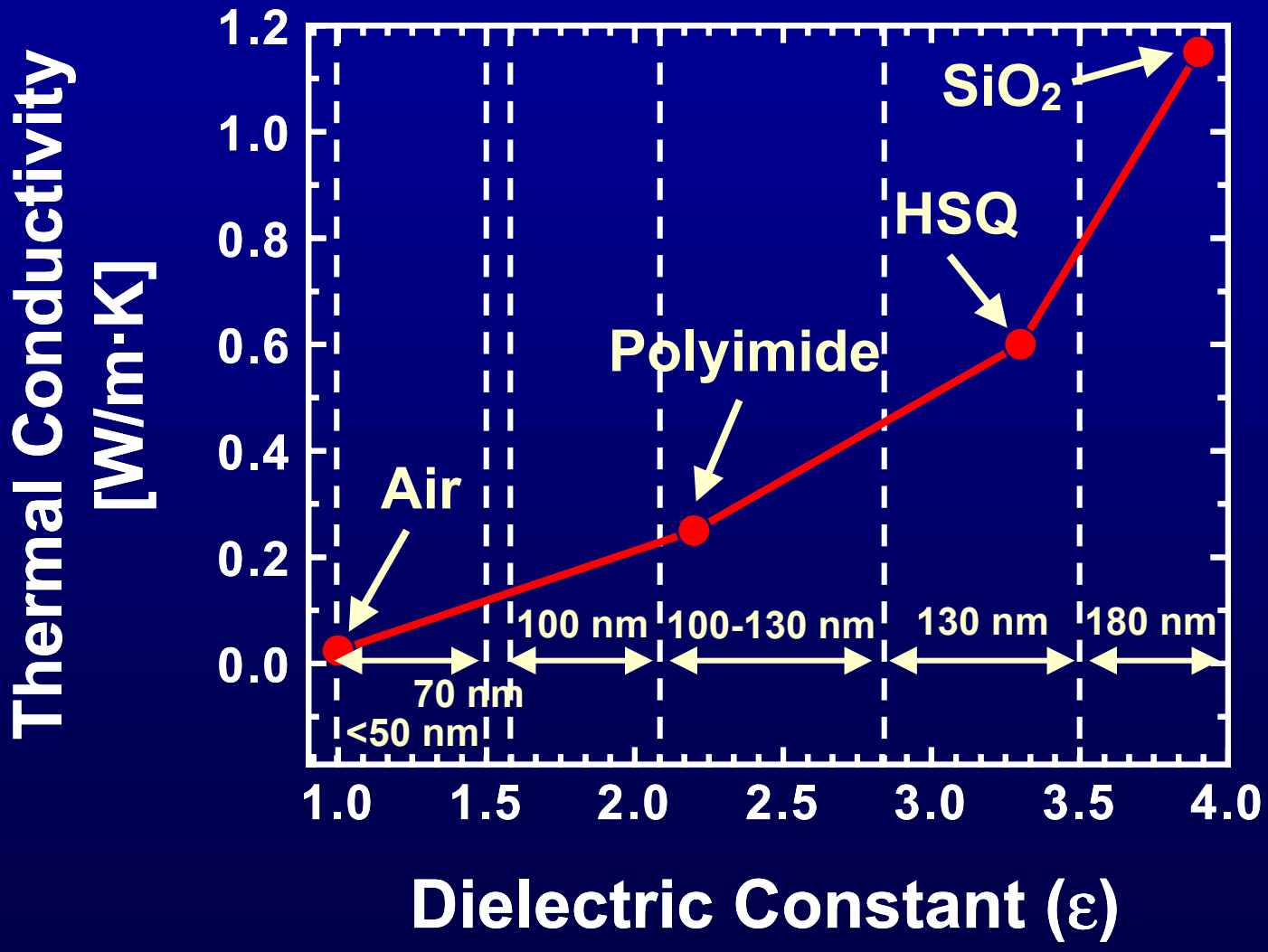
Presentation Outline

- Introduction
- Historical Perspective
- State-of-the-art in Modeling/Design
- Failure Mechanisms
- Summary
- Future Directions
- References

Introduction

- **Interconnect Failure under ESD Conditions**
  - Interconnects in the I/O and ESD protection circuits are subjected to high current stress
  - Can lead to open circuit failures or latent damage
- **Impact of Scaling (ITRS '99)**
  - IC performance is wire limited
  - Number of I/O pins increases $\Rightarrow$ Ball Grid Array
  - Reduced flexibility in wire sizing and spacing
  - Introduction of low-k dielectrics with lower thermal conductivity
  - Interconnect failure becomes more critical

Scaling Effects:
Thermal Conductivity of Dielectrics



(ITRS '99)

Historical Perspective

- Kinsborn et al. (1979)
  - conducted lifetime measurements of unpassivated Al conductors under continuous high current density pulses
  - attributed interconnect failure to a combination of electromigration, temperature cycling and chemical reaction between Al and SiO2
- Pierce (1982)
  - proposed a theoretical model for unpassivated metallization burnout under electrical overstress
  - assumed failure to occur at the melting point of metal

Historical Perspective

- Kim and Sachse (1991)
  - studied fracture strength of unpassivated metal lines deposited on window grade quartz substrates for a single shot current pulse
  - found temperature to initiate fracture in Al films to be around 300 ^{0}C
- Maloney (1992)
  - used passivated AlSi and AlCu and attributed failure to a combination of melting and evaporation
  - calculation of temperature rise based on adiabatic assumption

Historical Perspective

- **Murguia and Bernstein (1993)**
  - derived a simple relationship between the critical current density (j) to cause failure under short current pulses and the pulse width (t):
    - $j^2t = 10^8\ A^2s/cm^4$
  - based on the failure temperature of 300 ^{0}C and adiabatic conditions
- **Gui et al. (1995)**
  - carried out detailed simulations for passivated multilayered interconnect heating under transient stress conditions
  - demonstrated limitations of the adiabatic model for pulse widths > 2μs

Historical Perspective

- Ramaswamy et al. (1995)
  - reported interconnect damage in ESD protection circuits for advanced CMOS technology
- Banerjee et al. (1996, 1997)
  - developed transient resistive thermometry to estimate the temperature rise of AlCu wires
  - reported open circuit metal failure at 1000 ^{0}C
  - proposed a new interconnect heating model under ESD conditions
  - reported a latent interconnect damage that degrades EM lifetime
  - characterized the impact of low-k dielectrics

Historical Perspective

- Voldman (1997, 1998)
  - studied high current failure of Cu interconnects
  - showed that the Banerjee model can also be applied to damascene Cu interconnects
  - found Cu interconnects to be more robust than AlCu
- Salome et al. (1998)
  - confirmed the critical temperature rise of 1000 ^{0}C using SPICE based electrothermal simulations
  - confirmed the latent interconnect damage phenomenon

Historical Perspective

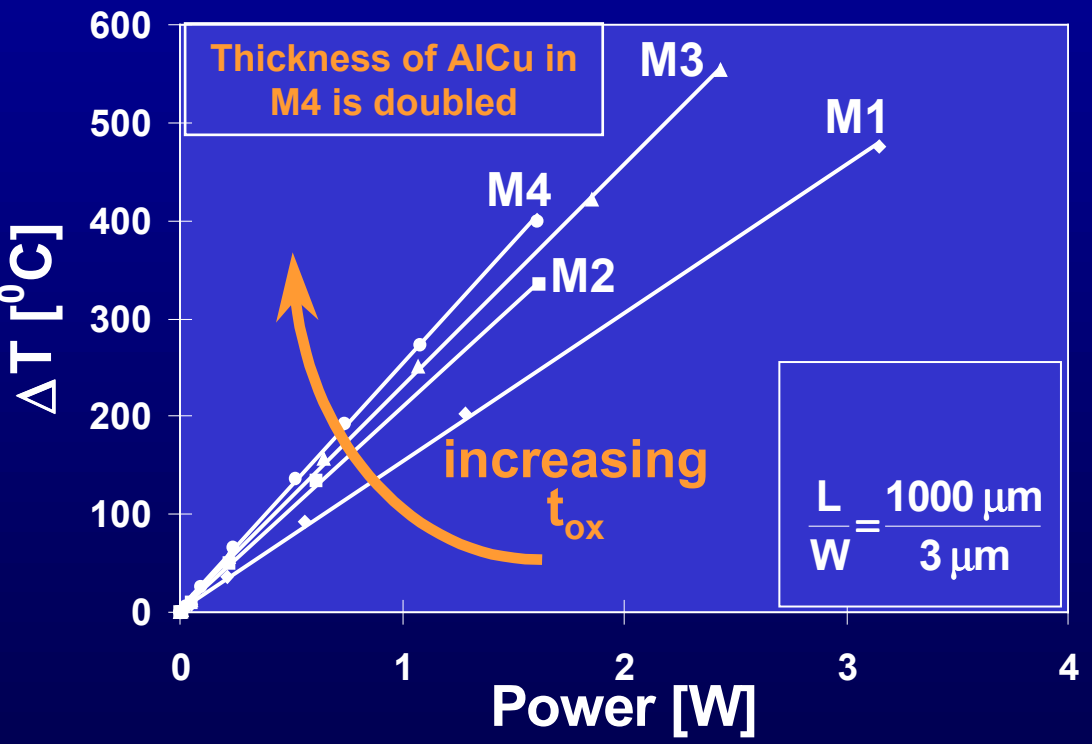
- **Banerjee et al. (2000)**
  - performed microanalysis of interconnect (AlCu) failure modes under ESD conditions
  - formulated a thermo-mechanical model to account for the open circuit failure
  - provided direct evidence of latent interconnect damage

EM vs Short-Pulse Failure

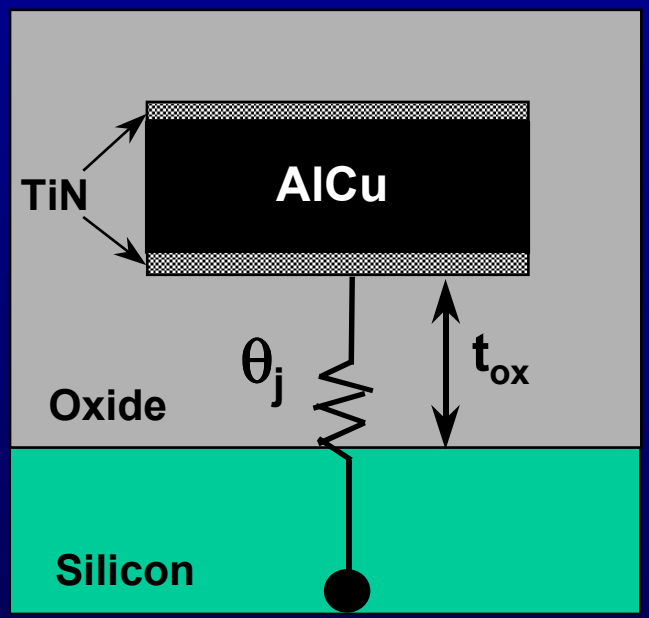
	J (A/cm^2)	Temperature (^0C)	Mechanism	Time scale
EM Failure				
Field Conditions:	$4 - 6 \times 10^5$	~ 85 - 100	diffusion	$t >> \tau_0$ steady state
Package Level:	$1 - 3 \times 10^6$	~ 100 - 200	diffusion	
Wafer Level:	$0.5 - 1 \times 10^7$	~ 150 - 300	diffusion	
High-Current Short-Pulse Failure	$> 10^7$	~ 1000	fusion	$t << \tau_0$ non-steady state

τ_0: thermal time constant (~ 2 μs)

Interconnect Heating under DC Stress (IRPS 96)



Cross section

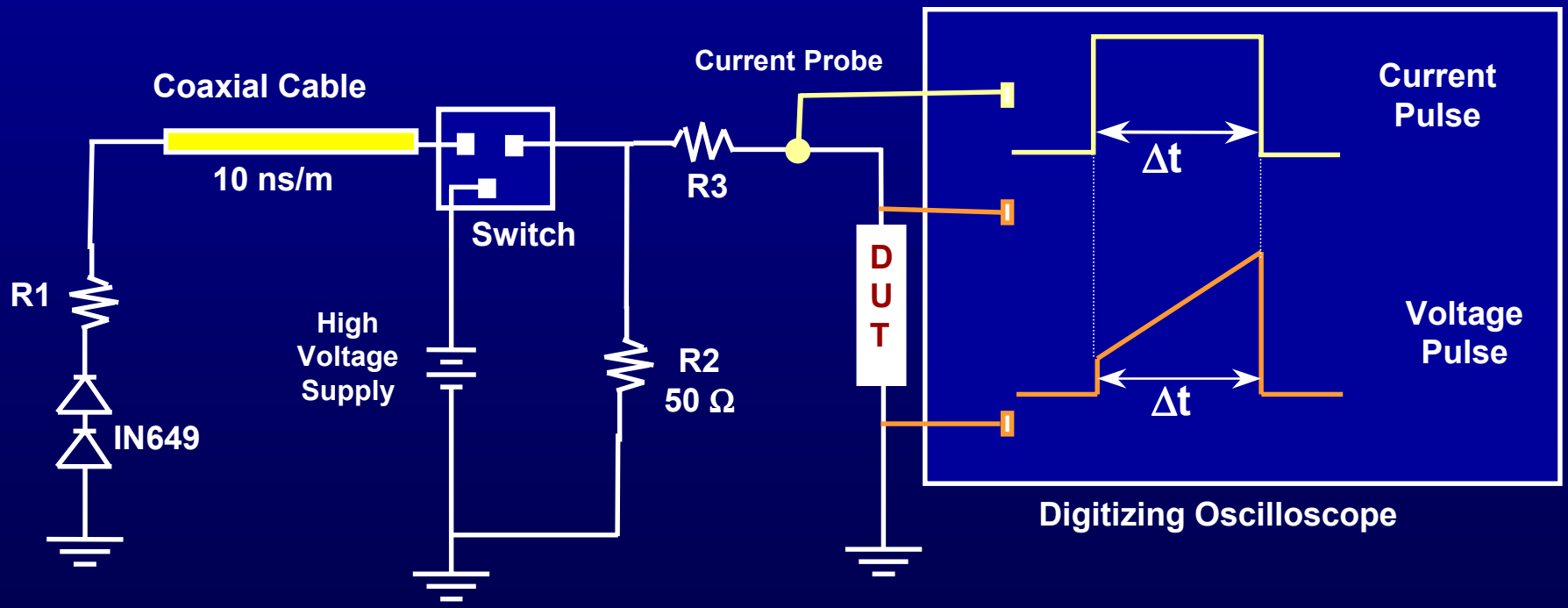


Thermal impedance θ_j, defined by $\Delta T = P \times \theta_j$

- ΔT increases with increasing t_{ox}

Transient Thermometry Measurement

- *Transmission Line Pulser System*



(IRPS 96)

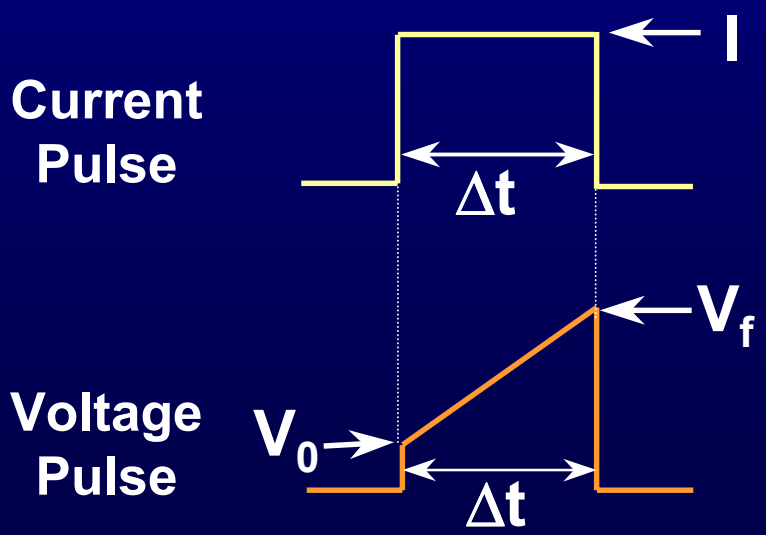
Experimental Approach

- ***DC Resistance Thermometry***

Temperature Rise, $$\Delta T = \left[\frac{R_f - R_0}{R_0}\right]\frac{1}{TCR}$$

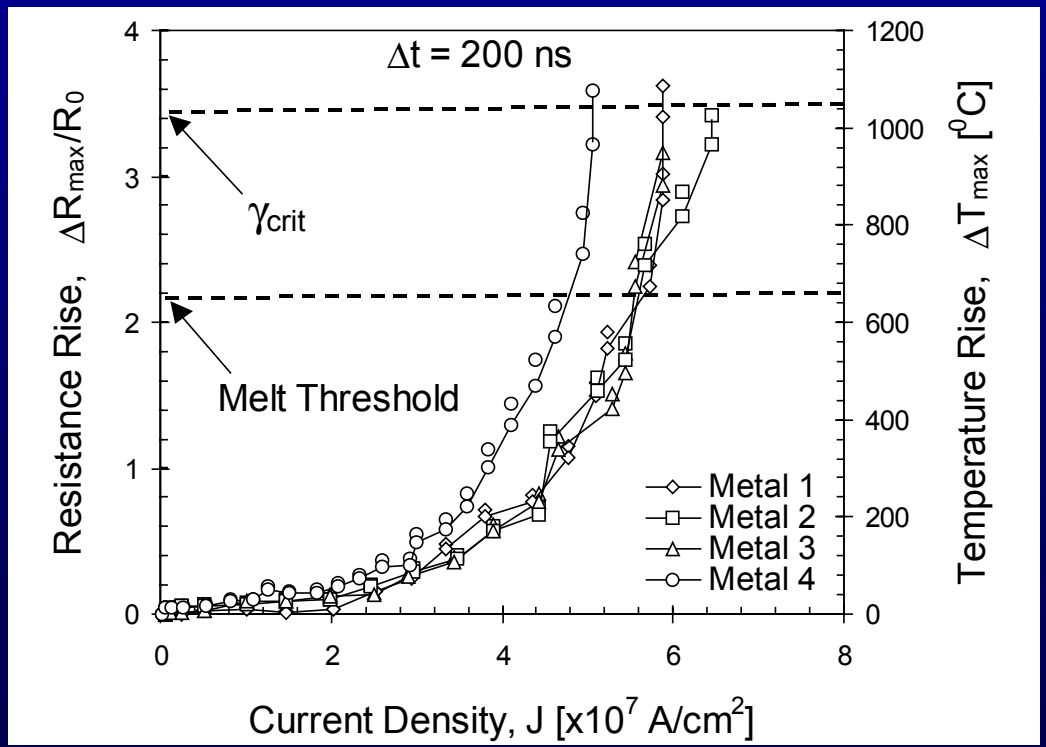
- **TCR is the temperature coefficient of resistance.**

- ***Transient Resistive Thermometry*** **(IRPS 96)**



Non Steady-State Self-Heating

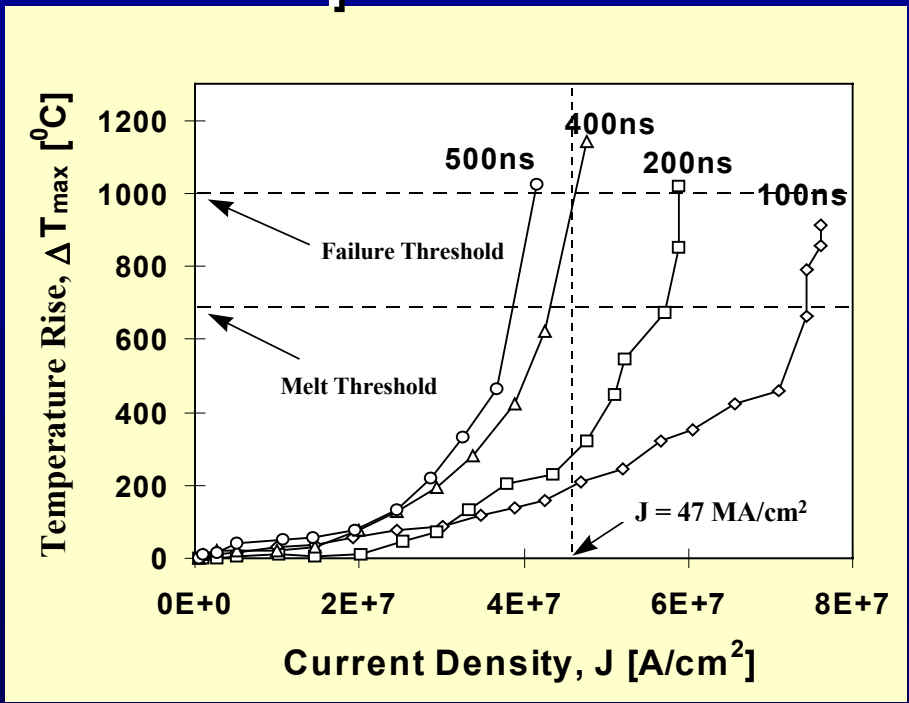
- Self-heating (SH) characteristics of AlCu lines under short-pulse stress conditions (EDL 97)



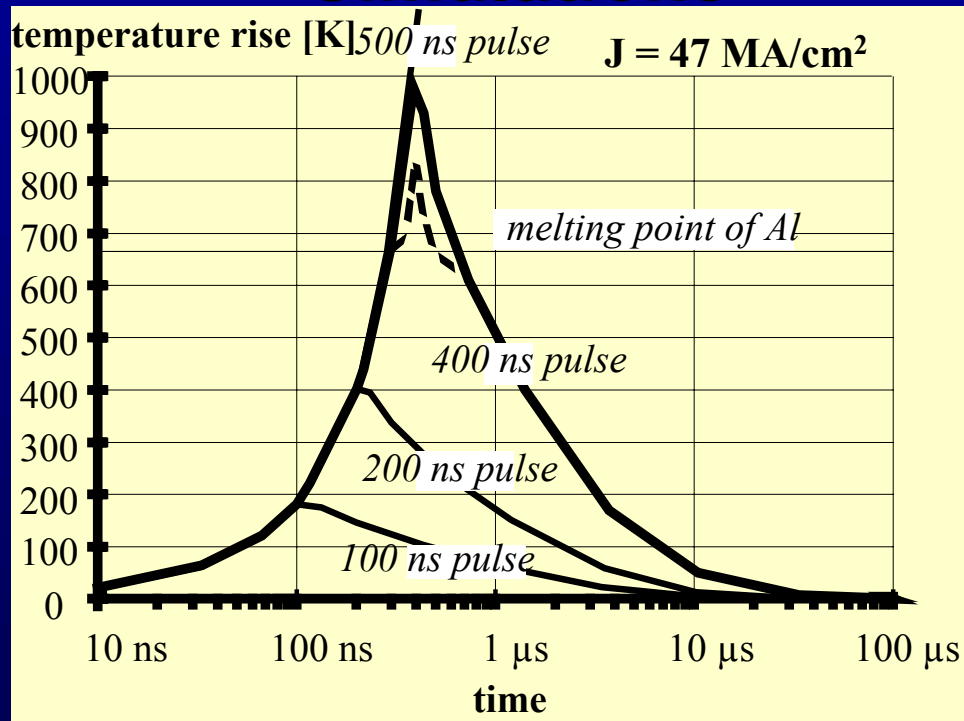
- Metal 1, 2, & 3 show identical SH
- Higher SH in Metal 4 is due to smaller surface area to volume ratio
- Interconnect failure temperature is ~ 1000 ^{0}C

Temperature Rise using Finite Element Simulations (IRW 96)

Experimental



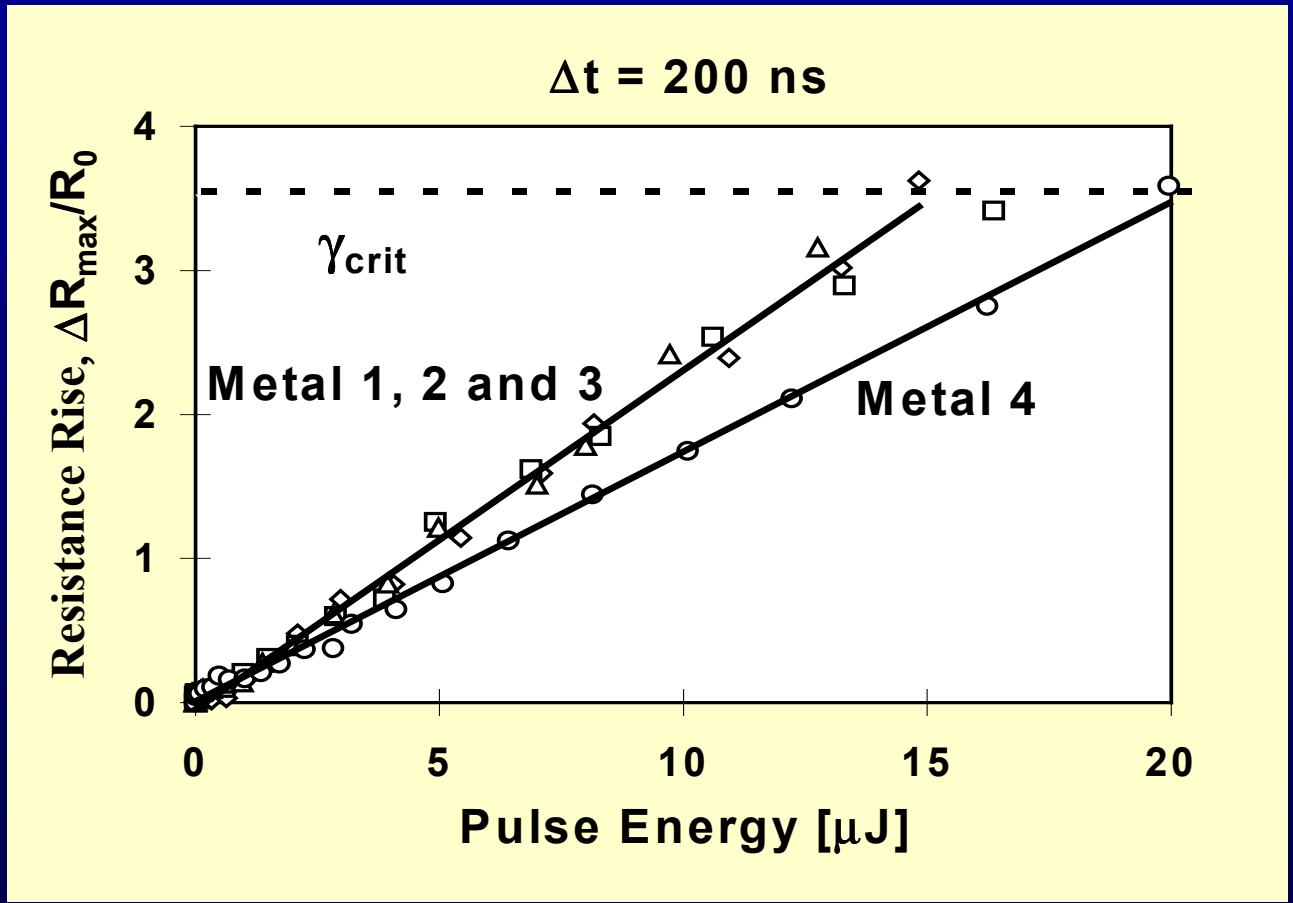
Simulations



- FE simulations confirm temperature rise beyond melting point.

Thermal Capacity under Short-Pulse Stress

(EDL 97)

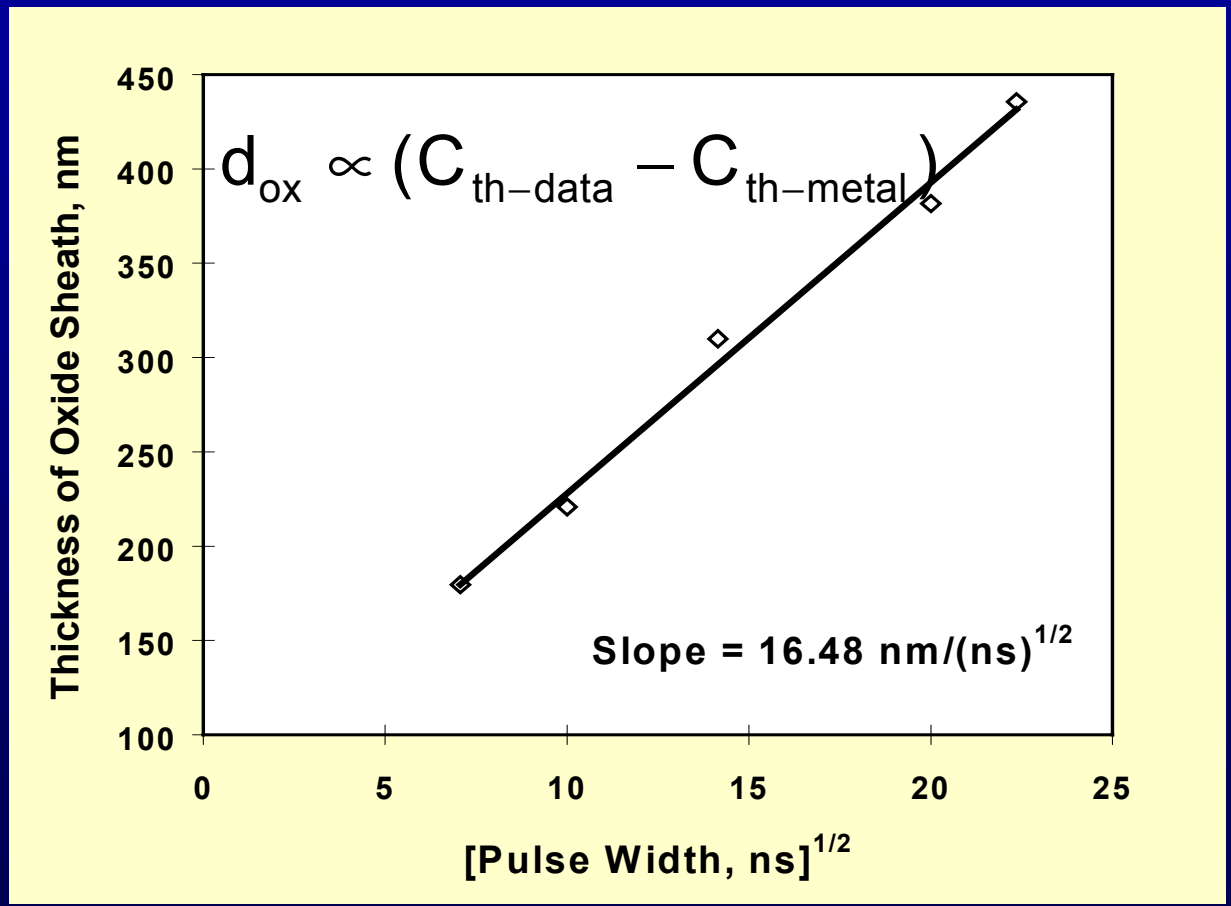


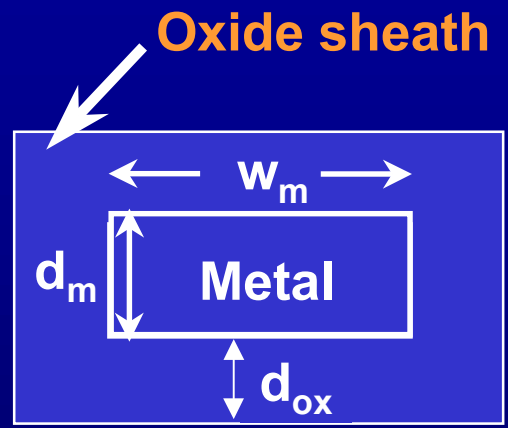
Pulse Energy

$$E = C_{th} \cdot \Delta T = C_{th} \cdot \left(\frac{R_f - R_0}{R_0}\frac{1}{TCR}\right)$$

C_{th} = thermal capacity

Oxide Sheath Model (EDL 97)





From heat diffusion theory

$$d_{ox} = \sqrt{a_d t}$$

- Difference in extracted and calculated thermal capacity is used to calculate the oxide sheath thickness

Energy Considerations

(EDL 97)

Pulse energy: $E = \int_0^{\Delta t} I \cdot V dt$

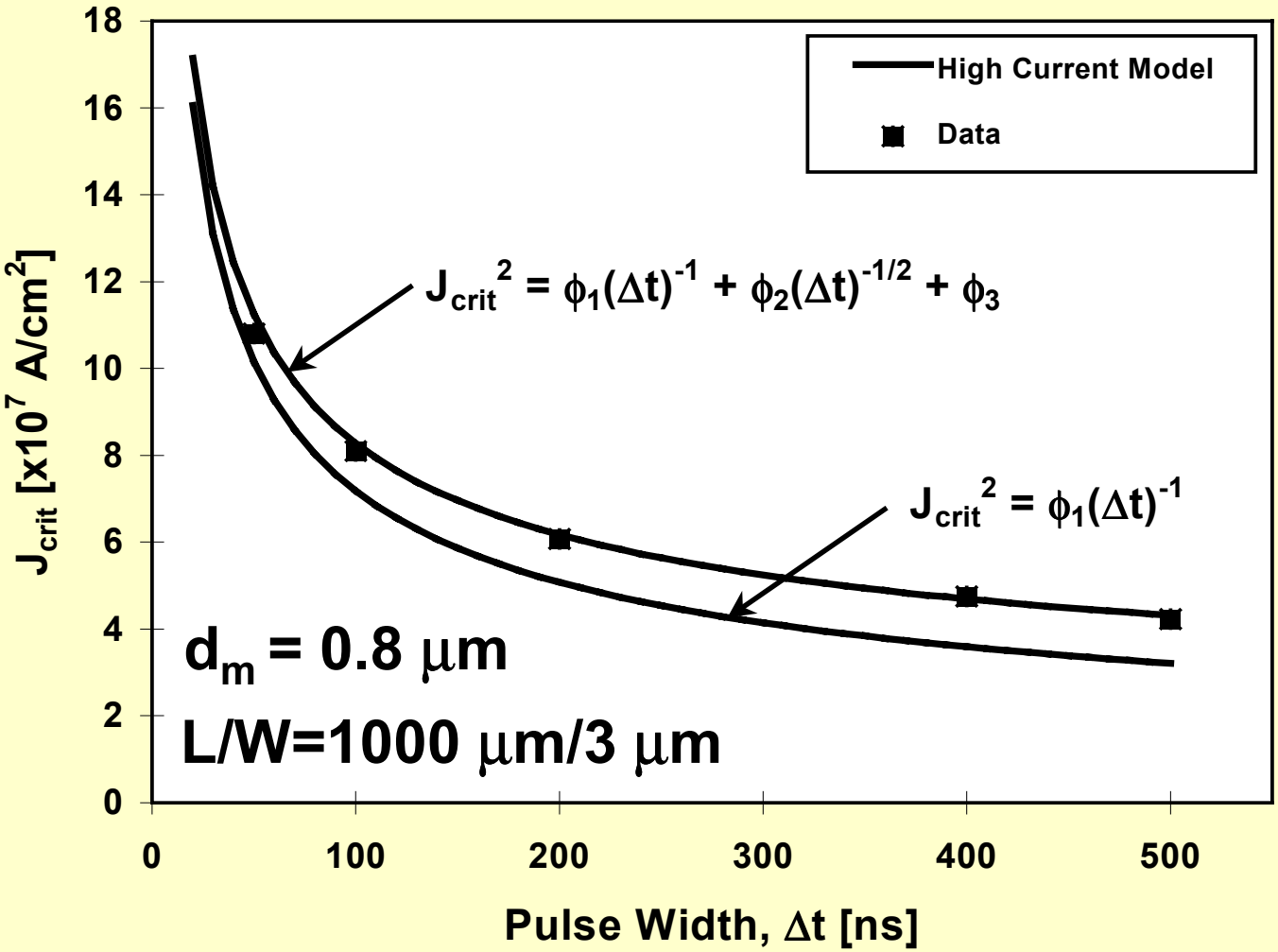
$$E_{critical} = \left[C_{AlCu} + C_{TiN} + C_{oxide-sheath} \right] \Delta T_{critical} + E_{Melt}$$

$$\Rightarrow J^2_{critical} = \Phi_1 \, \Delta t^{-1} + \Phi_2 \, \Delta t^{-1/2} + \Phi_3$$

(adiabatic) (heat diffusion)

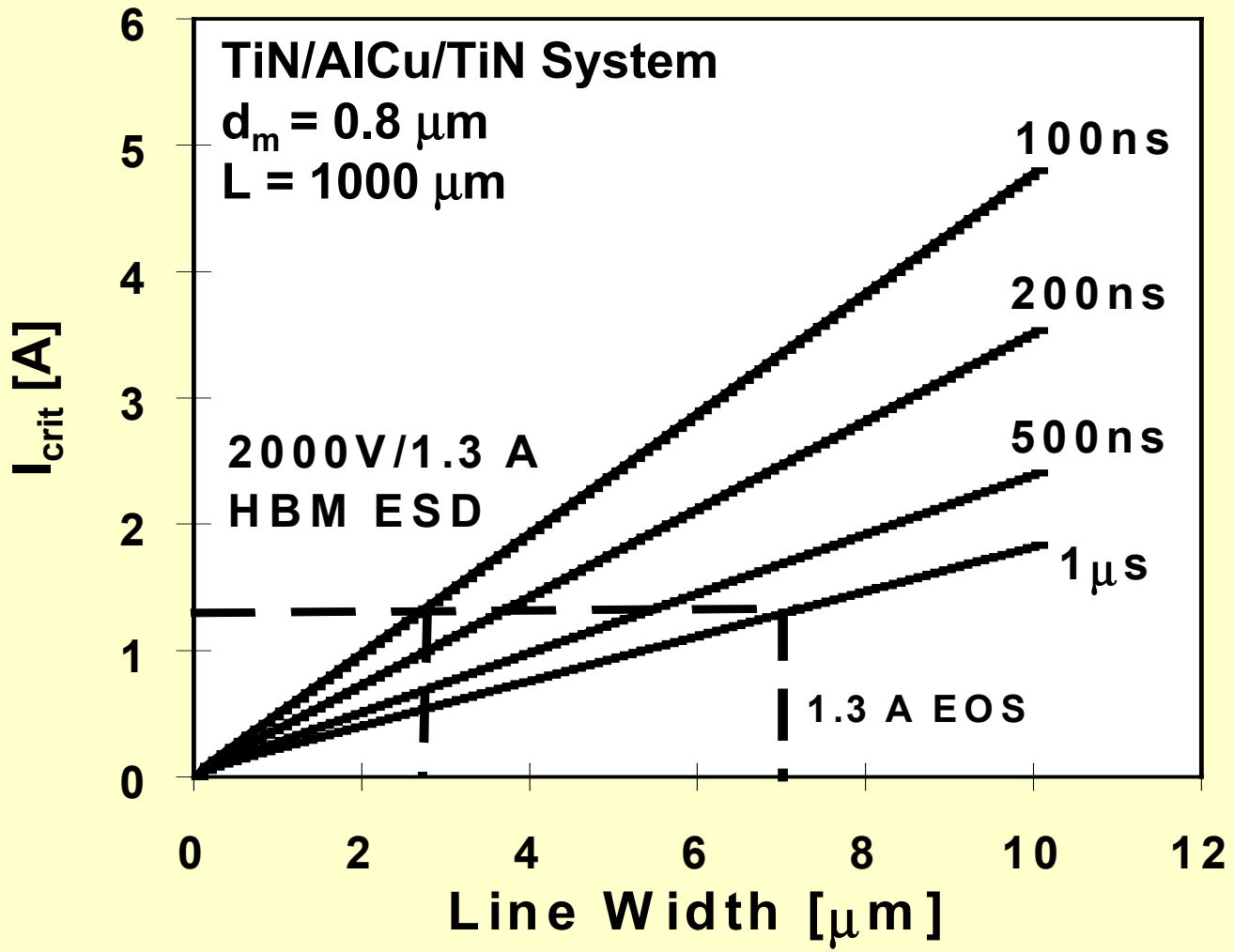
Maximum Current Density Model

(EDL 97)



High Pulsed-Current Design Rules

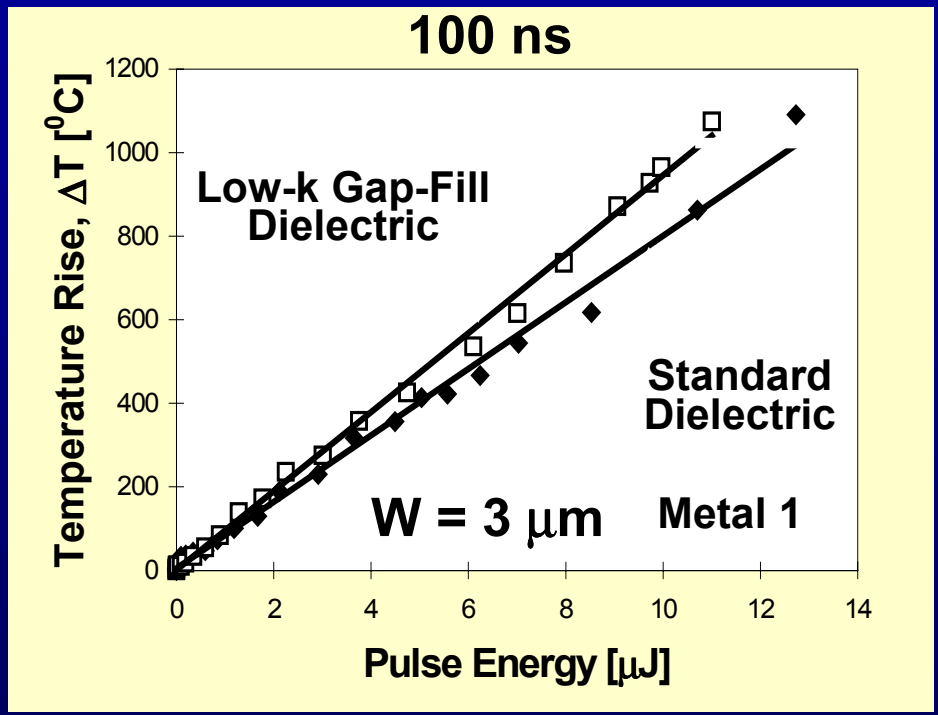
(EDL 97)

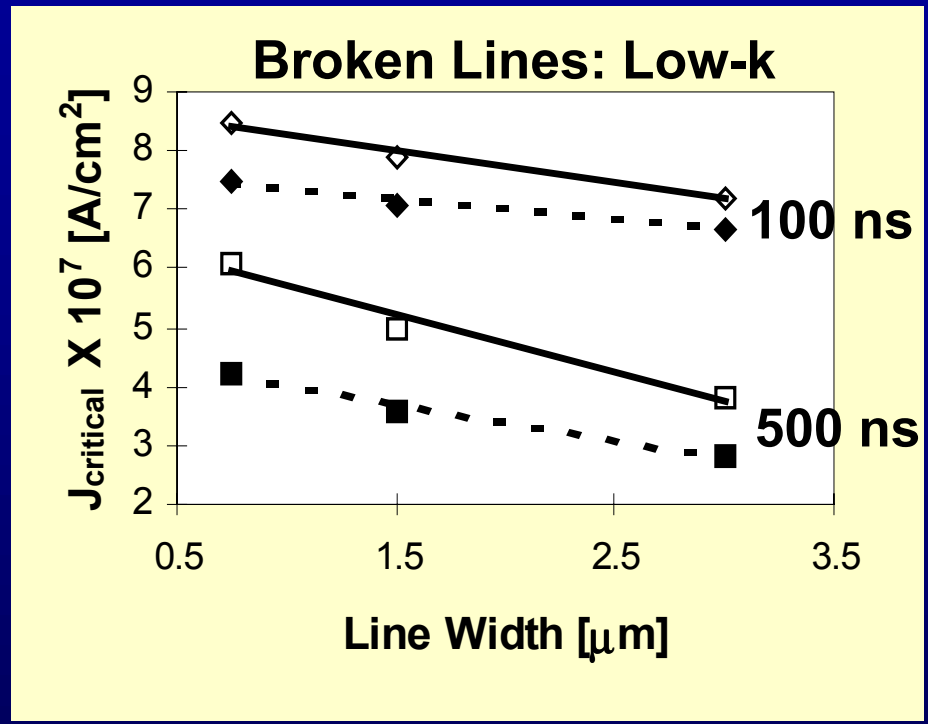


Impact of Line Width Scaling and Low-k

Pulsed Conditions

(IEDM 96)





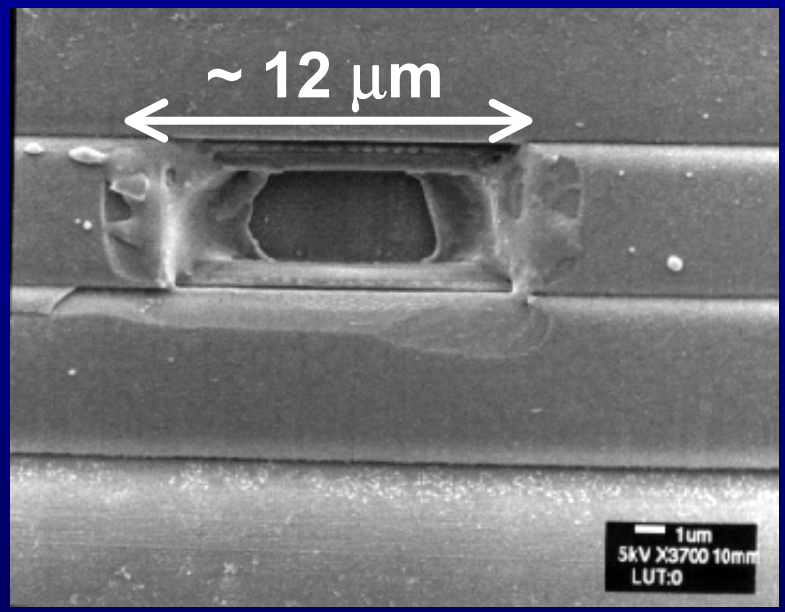
- Low-k - smaller thermal capacity due to lower thermal conductivity
- As W decreases and pulse width increases effect of low-k increases

Summary (1)

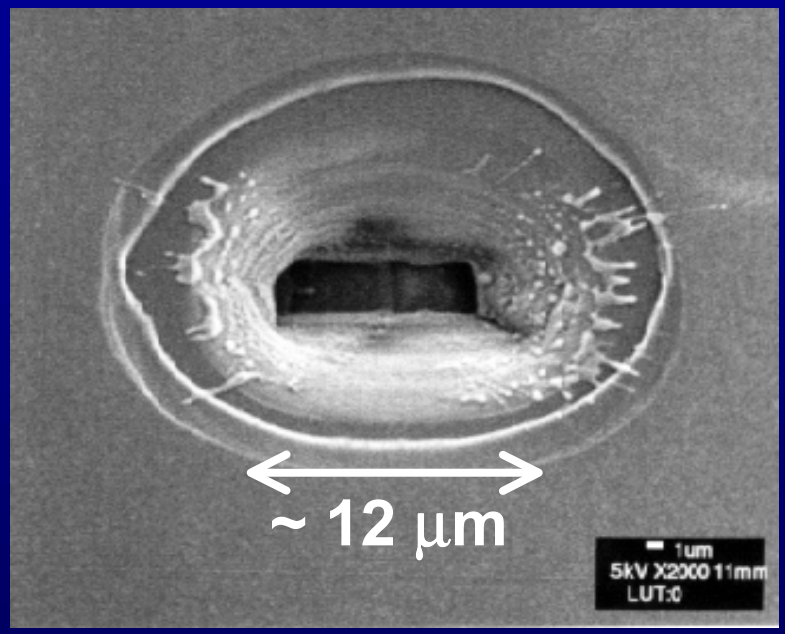
- Interconnect heating under short pulses - not entirely adiabatic - strongly dependent on the thermal capacity of the metal, the pulse width, and the surrounding dielectric material.
- Oxide Sheath Model: A new technique to estimate thermal conductivity of low-k dielectrics.
- Line width scaling and low-k dielectric impacts interconnect heating.
- High current/ESD metal design guidelines generated.

Open Circuit Failures

(IRPS 2000)



Metal 4

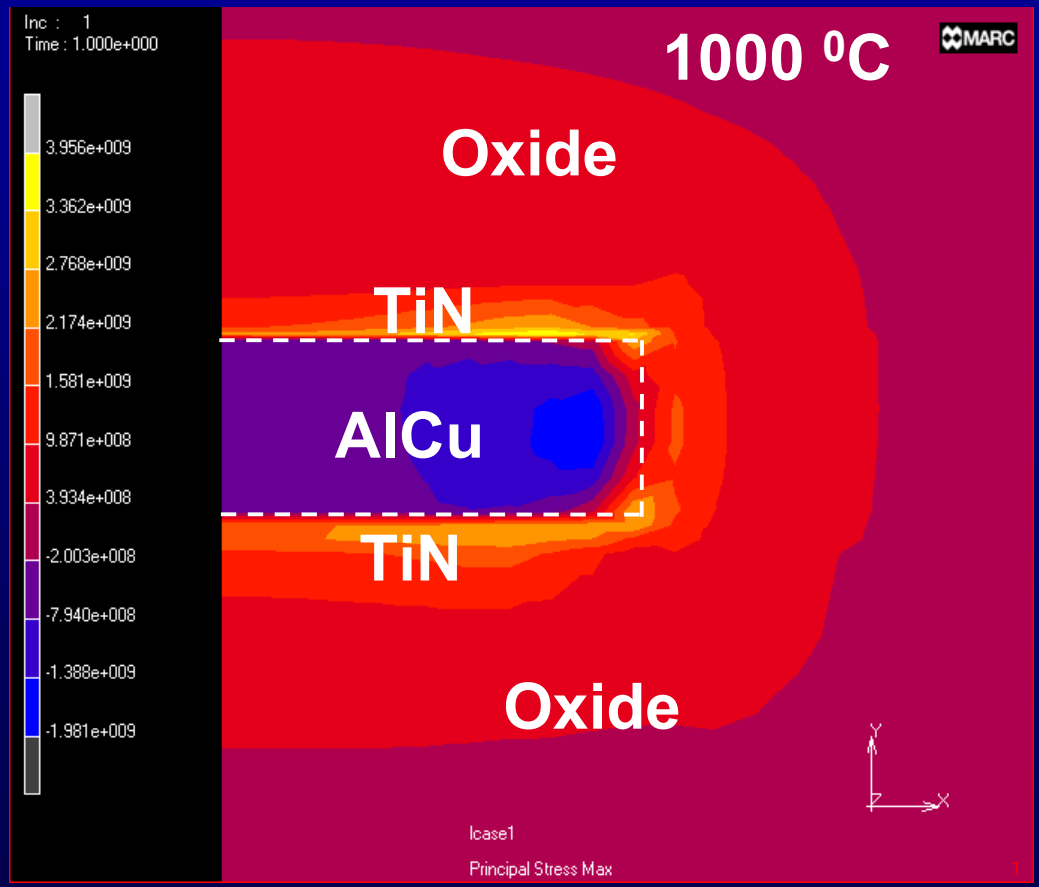


Metal 1

- Passivation fracture due to the expansion of critical volume of molten AlCu. (@ 1000 ^{0}C)
- Independent of overlying dielectric thickness

Thermomechanical Simulation (IRPS 2000)

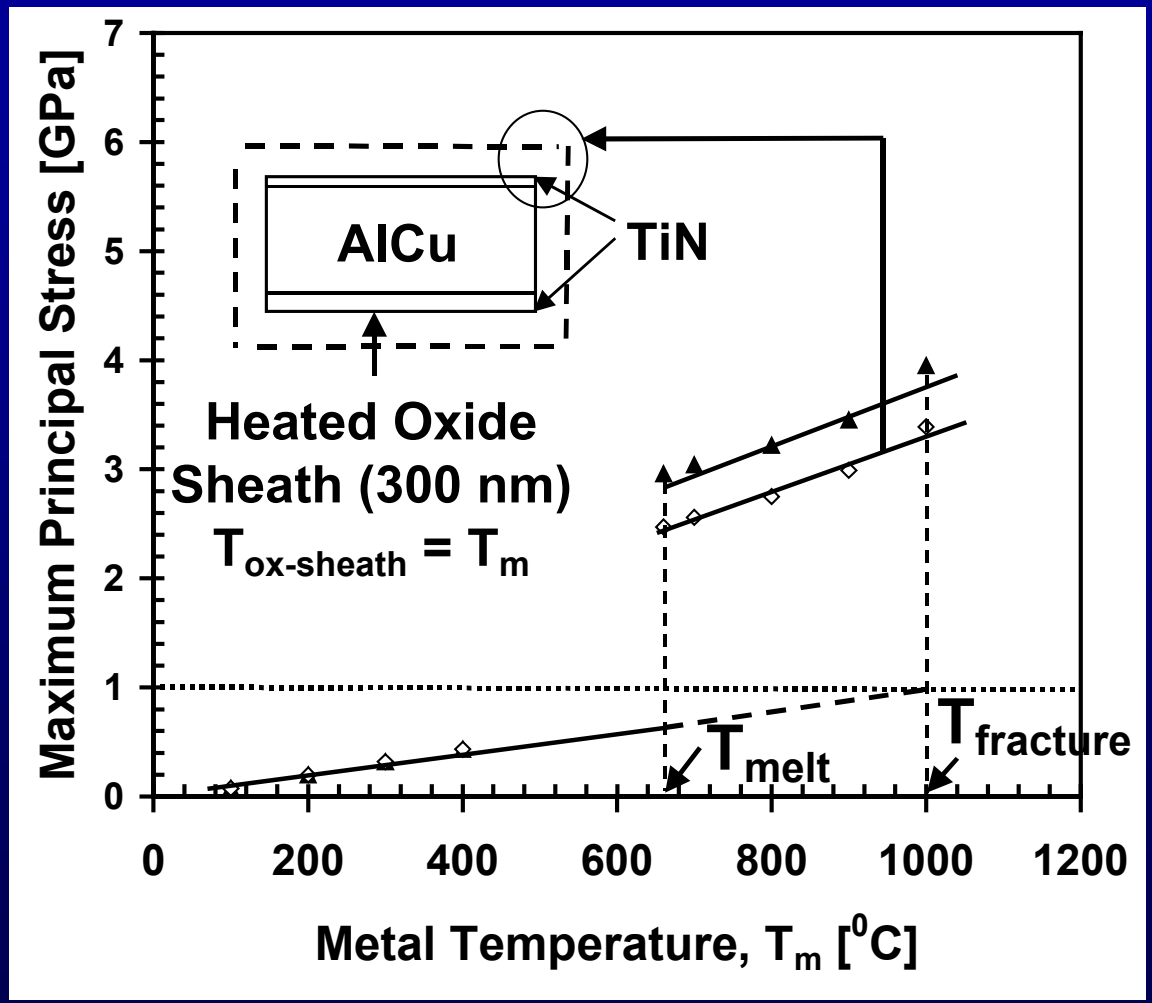
Stress States



- Oxide sheath under higher tensile stress

Stress States

(IRPS 2000)



Passivation fracture strength: ~ 1 GPa

- **Artificially high stresses beyond T_{melt} $\Rightarrow$ entire line does not melt at temperatures well beyond T_{melt}**

Latent Damage

- **Latent ESD Damage:** AlCu lines pulsed by sub-critical pulses show significant electromigration degradation without measurable change in line resistance. [Banerjee, *IRPS '96*]
- **Microstructure change** was proposed to explain the EM degradation without any physical evidence

Experimental

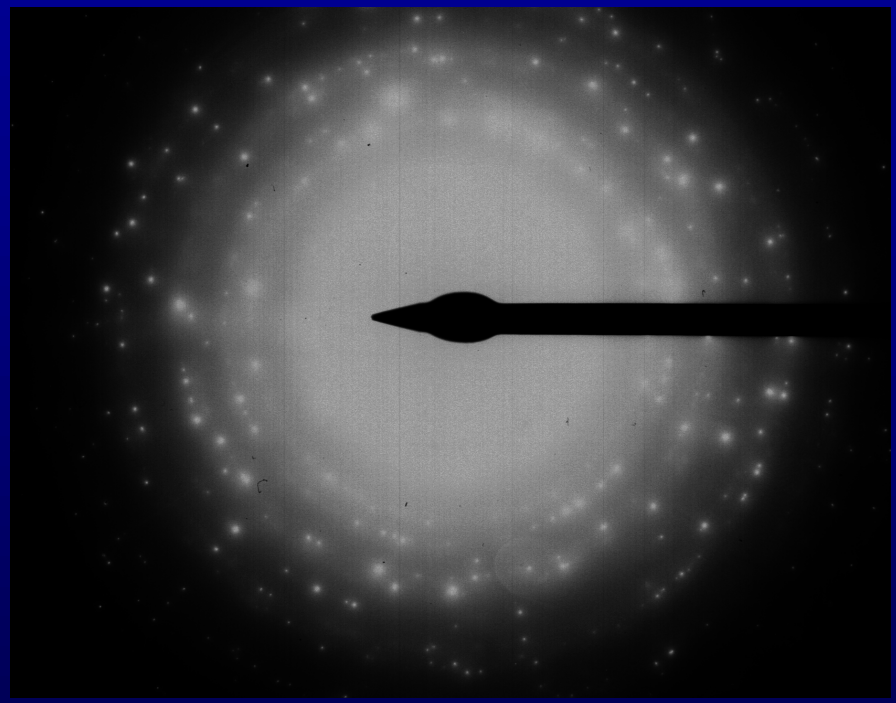
(IRPS 2000)

- Unstressed AlCu lines
- AlCu lines pulsed just below the open circuit failure temperature
  - No physical damage or increase in line resistance
  - EM lifetime degradation by a factor of 4

TEM Micrograph: Unstressed AlCu Line (IRPS 2000)

- Average grain size: 1.2 μm
- Well defined grain shape

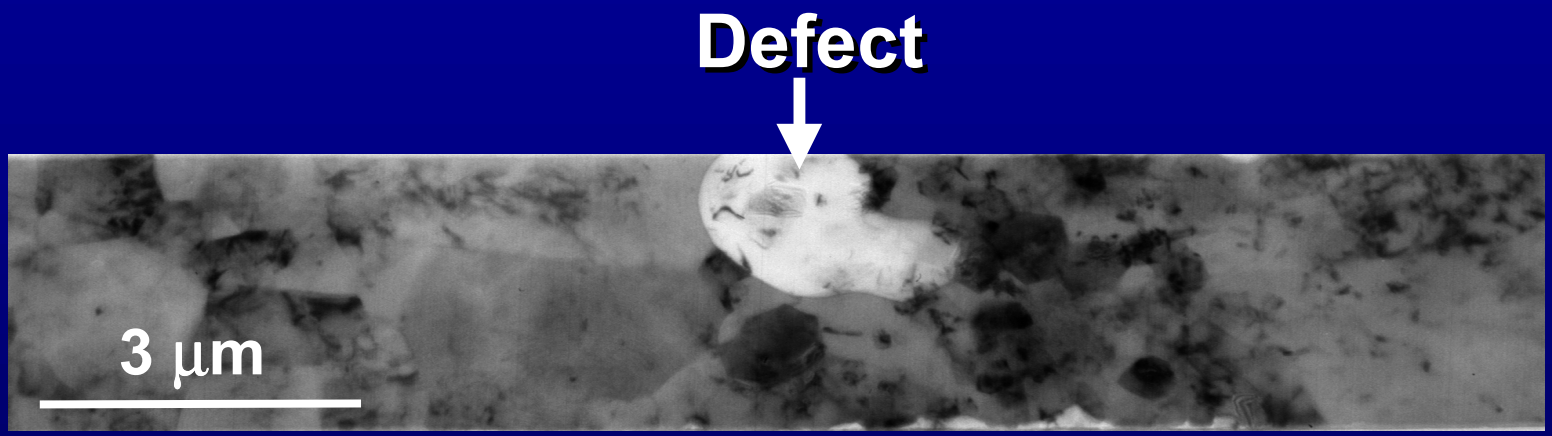
Diffraction Pattern: Unstressed AlCu Line (IRPS 2000)



- Sparse spatial formation of diffraction spots

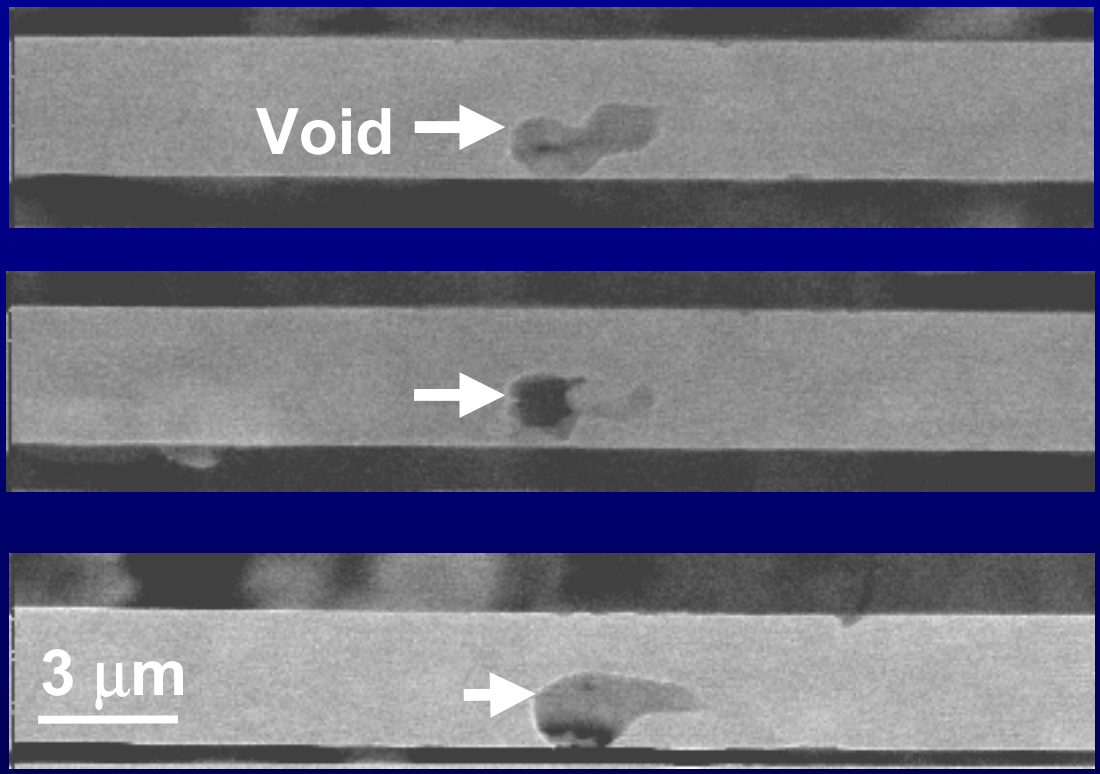
  ⇨ small number of large grains

TEM Micrograph: Stressed AlCu Line (IRPS 2000)



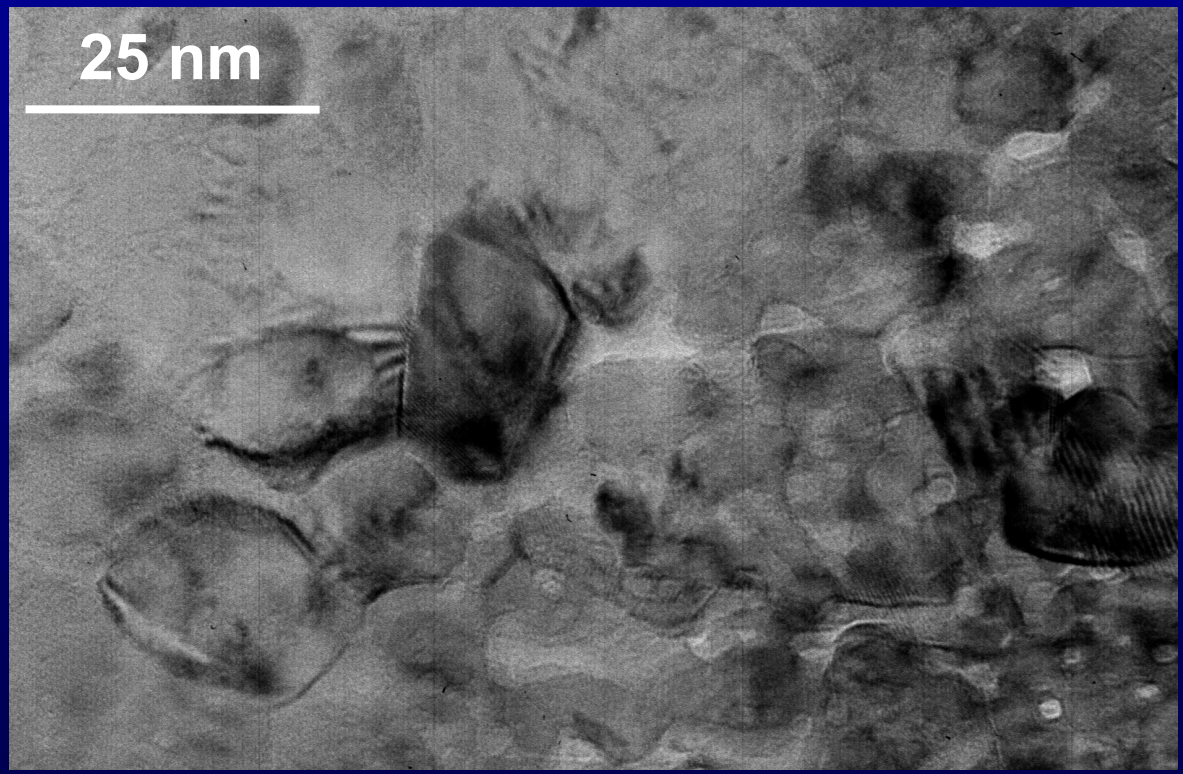
- Different microstructure (small grain size) around the spot ---melting and resolidification
- Segments between defects with grain size identical to unstressed line ---entire line does not melt

SEM Micrograph (IRPS 2000)



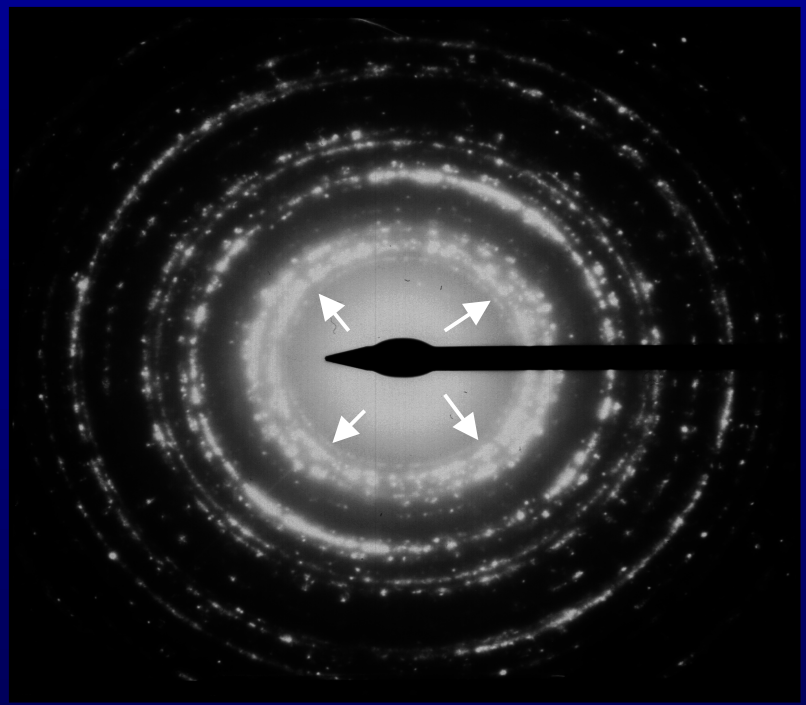
- Reveals material loss at the defect sites ---metal diffusion

TEM Micrograph: Microstructure Near the Defect (IRPS 2000)



- Reveals very small grain formation

Diffraction Pattern Near The Defect Site (IRPS 2000)



- Diffraction rings ⇨ large number of small grains
- Innermost ring ⇨ new phase, different from AlCu

Latent Failure Mechanism

- Void nucleation and growth result from diffusional processes under high current density and high temperature.
- Short duration of the pulse induces localized melting only.
- Small grains around the defects can only result from melting and resolidification.

Summary (2)

- Detailed microanalysis of passivated AlCu lines has provided direct evidence of latent metal damage causing EM degradation:
  - Voiding: due to material diffusion under high temperature and current density.
  - Grain size reduction: due to melting and resolidification.
- Thermo-mechanical model for open circuit failures explains the unusually high failure temperature.

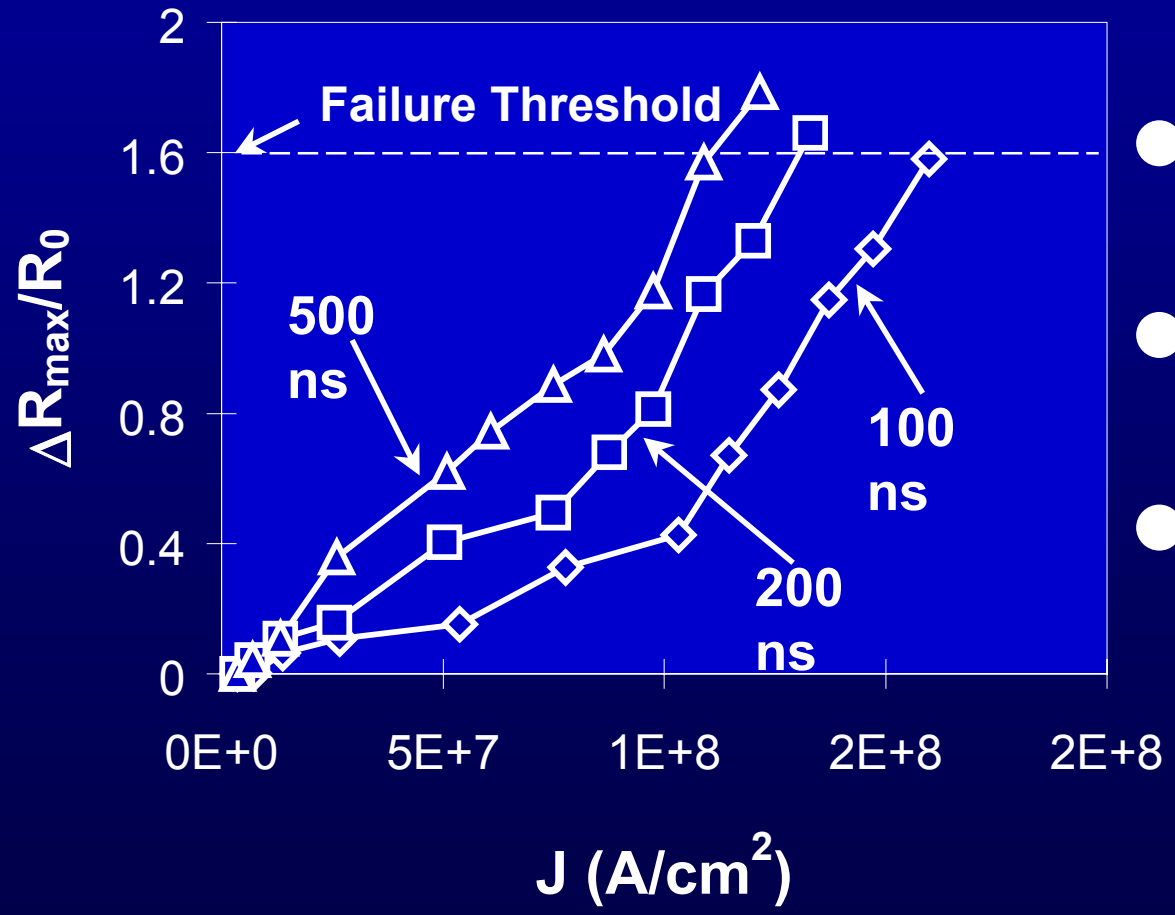
Contact and Via Characterization

Banerjee et al., IRPS 1997

- Characterized contact and via failure under short time joule heating (ESD events)
- Identified mechanisms responsible for contact/via degradation and failure under these stresses
- Presented a methodology to study effects of process variation on contact robustness

Self-Heating Characteristics for Single 0.3μm W-Contacts

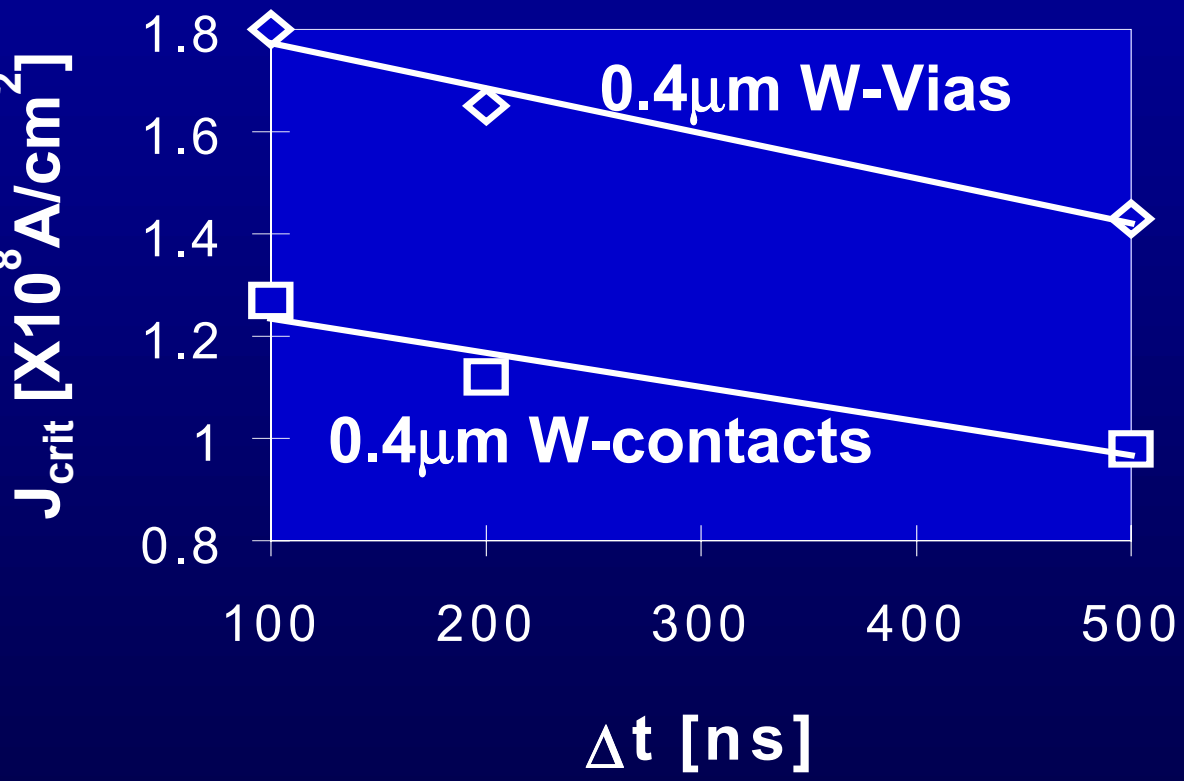
(IRPS 97)



- J_{crit} decreases with pulse width
- Independent of direction of current
- ΔT exceeds 800 ^0C

Contact and Via Robustness under Short Pulsed Stress

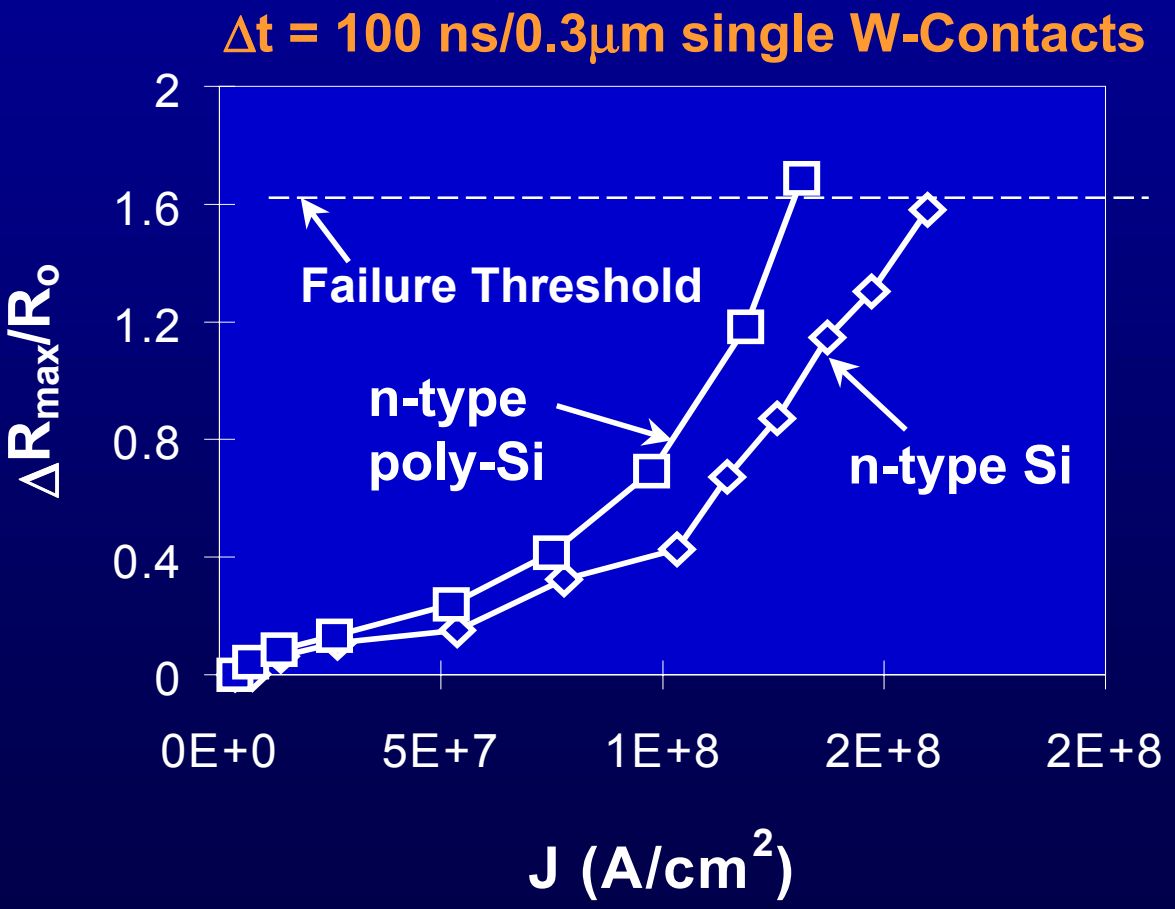
(IRPS 97)



- Vias are more robust due to their lower resistance and better heat conduction capability

Effect of Substrate Thermal Conductivity

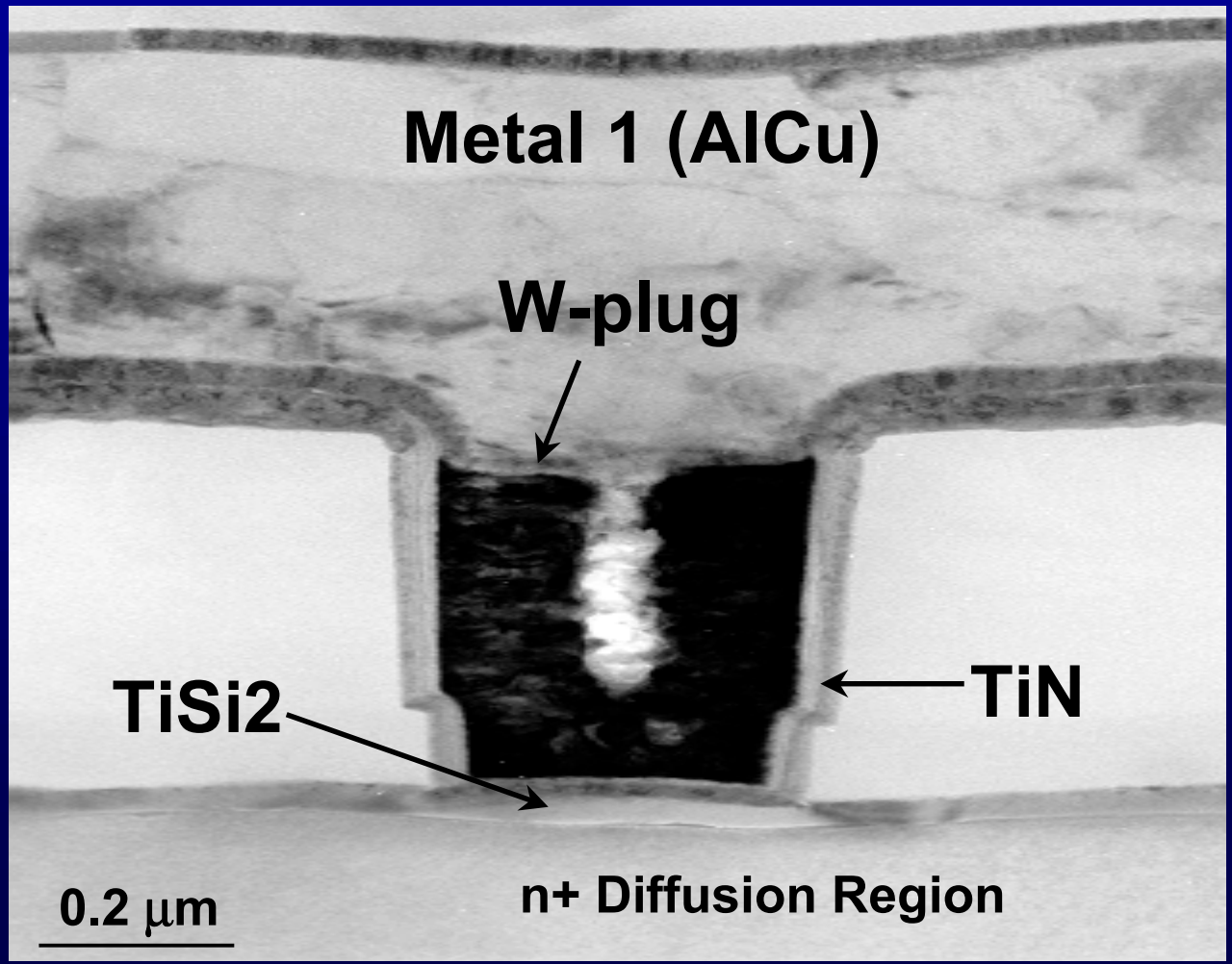
(IRPS 97)



- J_{crit} decreases for contacts to poly-Si
- Heat dissipation is less efficient for contacts to poly-Si

TEM of Unstressed W-Contact to n+ Si

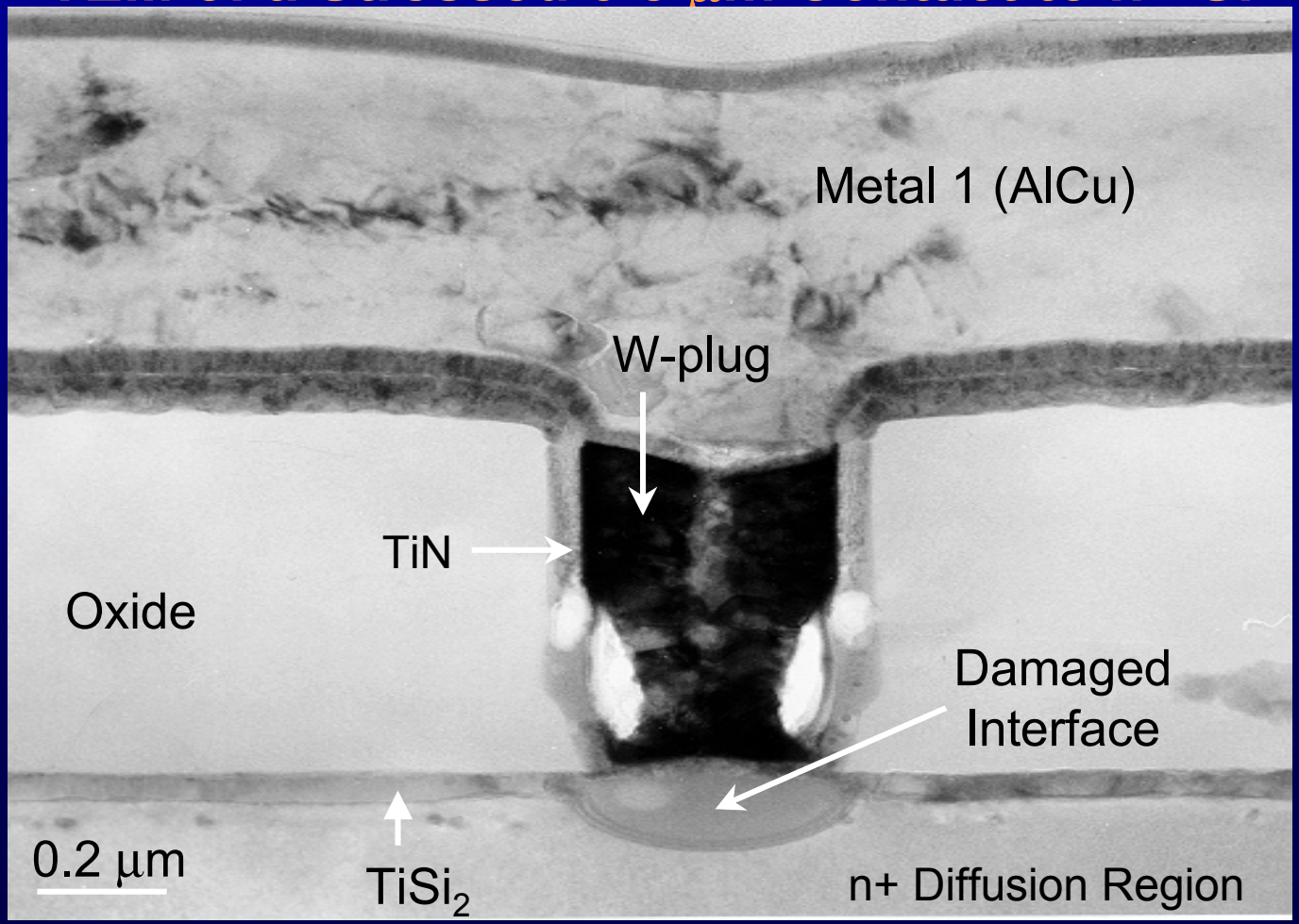
(IRPS 97)



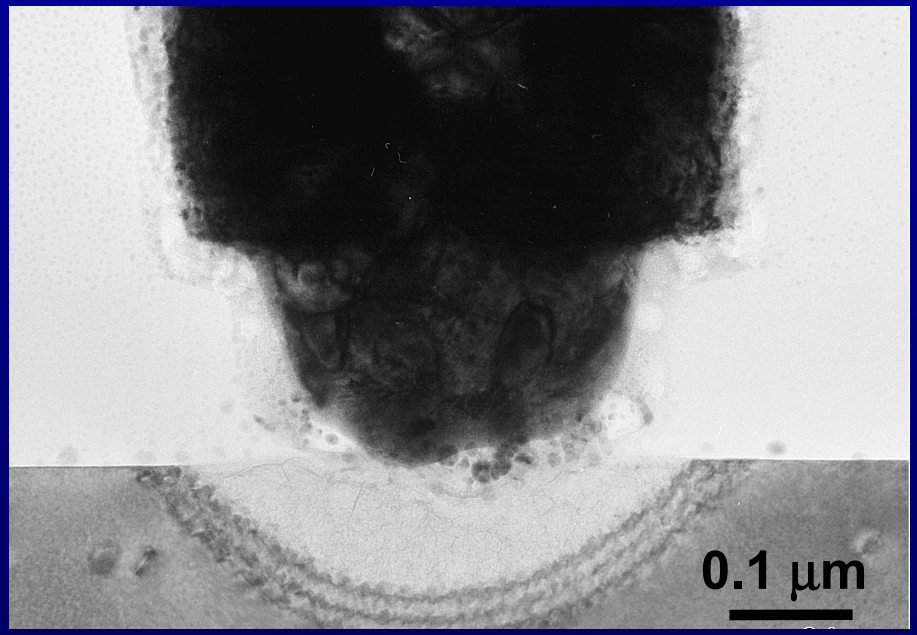
Silicided Contact Degradation

(IRPS 97)

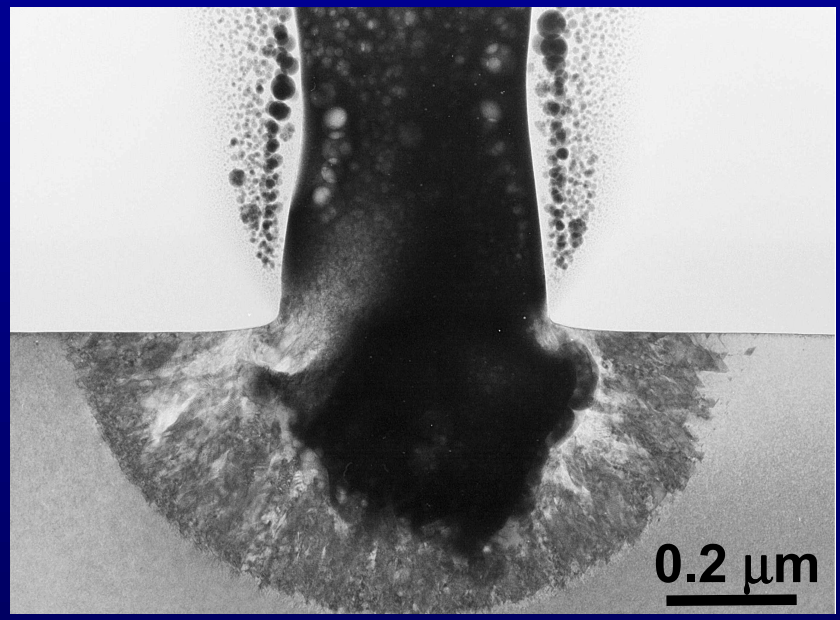
TEM of a Stressed 0.3 μm Contact to n+ Si



Evolution of Contact Degradation Under High Current Stress (IEDM 97)



Initial degradation state



Severe degradation state

- The degradation front is captured using a short pulse.

Summary (3)

- TEM analysis used to identify contact failure mechanism under short-pulse stress: characterized by a breakdown of the TiN/TiSi2 interface
- Contact degradation is independent of the current direction, plug material and sheet resistivity of the diffusion region
- Contact degradation sensitive to the thermal conductivity of the substrate
- J_{crit} has a strong dependence on the pulse width, cross sectional area and number of contacts

Future Directions

- Interconnect reliability due to high-current/ESD events will become increasingly important for deep sub-micron technologies
- Need to characterize lines, vias, contacts, and their interfaces involving emerging materials
- The transient resistive thermometry technique can be an effective tool for high-current characterization of various interconnect structures
- The transient technique is also very useful for studying various thermally accelerated interconnect failure mechanisms

References (1)

- K. Banerjee and A. Mehrotra, "Global (Interconnect) Warming," *IEEE Circuits and Devices Magazine*, September 2001.
- T-Y. Chiang, K. Banerjee, K. C. Saraswat, "Effect of Via Separation and Low-k Dielectric Materials on the Thermal Characteristics of Cu Interconnects," *IEDM*, 2000, pp. 261-264.
- K. Banerjee, D. Y. Kim, A. Amerasekera, C. Hu, S. S. Wong, and K. E. Goodson, "Microanalysis of VLSI Interconnect Failure Modes under Short-Pulse Stress Conditions," *IRPS*, 2000, pp. 283-288.
- S. H. Voldman, "The Impact of Technology Scaling on ESD Robustness of Aluminum and Copper Interconnects in Advanced Semiconductor Technologies," *IEEE Trans. Components, Packaging, and Manufacturing Technology*-Part C, Vol. 21, No. 4, pp. 265- 277, 1998.
- P. Salome, C. Leroux, P. Crevel, and J. P. Chante, "Investigations on the Thermal Behavior of Interconnects under ESD Transients using a Simplified Thermal RC Network," *EOS/ESD Symp. Proc.*, 1998, pp. 187-198.
- K. Banerjee, A. Amerasekera, J. A. Kittl, and C. Hu, "High Current Effects in Silicide Films for Sub-0.25 micron VLSI Technologies," *IRPS*, 1998, pp. 284-292.
- K. Banerjee, A. Amerasekera, G. Dixit, and C. Hu, "Temperature and Current Effects on Small-Geometry-Contact Resistance," *IEDM*, 1997, pp.115-118.
- S. H. Voldman, "ESD Robustness and Scaling Implications of Aluminum and Copper Interconnects in Advanced Semiconductor Technology," *EOS/ESD Symp. Proc.* 1997, pp. 316-329.
- K. Banerjee, A. Amerasekera, N. Cheung, and C. Hu, "High-Current Failure Model for VLSI Interconnects Under Short-Pulse Stress Conditions," *IEEE Electron Device Letters*, vol. 18, No. 9, pp. 405-407, 1997.
- K. Banerjee, A. Amerasekera, G. Dixit, N. Cheung, and C. Hu, "Characterization of Contact and Via Failure under Short Duration High Pulsed Current Stress," *IRPS*, 1997, pp. 216-220.

References (2)

- K. Banerjee, S. Rzepka, A. Amerasekera, N. Cheung, and C. Hu, "Thermal Analysis of the Fusion Limits of Metal Interconnect under Short Duration Current Pulses," *IRW*, 1996, pp. 98-102.
- K. Banerjee, A. Amerasekera, G. Dixit, and C. Hu, "The Effect of Interconnect Scaling and Low-k Dielectric on the Thermal Characteristics of the IC Metal," *IEDM*, 1996, pp. 65-68.
- K. Banerjee, A. Amerasekera, and C. Hu, "Characterization of VLSI Circuit Interconnect Heating and Failure under ESD Conditions," *IRPS*, 1996, pp. 237-245
- S. Ramaswamy, C. Duvvury and S. Kang, "EOS/ESD Reliability of Deep Sub-micron NMOS Protection Devices," *IRPS*, 1995, pp. 284-291.
- X. Gui, S. D. Dew and M. J. Brett, "Thermal Simulation of Thin-film Interconnect Failure Caused by High Current Pulses," *IEEE Trans. Electron Devices*, Vol. 42, No. 7, pp. 1386-1388, 1995.
- J. E. Murguia and J. B. Bernstein, "Short-time Failure of Metal Interconnect Caused by Current Pulses," *IEEE Electron Device Lett.*, Vol. 14, No. 10, pp. 481-483, 1993.
- T. J. Maloney, "Integrated Circuit Metal in the Charged Device Model: Bootstrap Heating, Melt Damage and Scaling Laws," *EOS/ESD Symp. Proc.*, 1992, pp. 129-134.
- K. Y. Kim and W. Sachse, "Dynamic Fracture Test of Metal Thin Films Deposited on an Insulating Substrate by a High Current Pulse Method," *Thin Solid Films*, 205, pp. 176-181, 1991.
- D. G. Pierce, "Modeling Metallization Burnout of Integrated Circuits," *Proc. EOS/ESD Symp.*, 1982, pp. 56-61.
- E. Kinsborn, C. M. Melliar-Smith, and A. T. English, "Failure of Small Thin-film Conductors due to High Current Density Pulses," *IEEE Trans. Electron Devices*, vol ED-26, No. 1, pp. 22-26, 1979.